**Goal: User-friendly Reconfiguration**

**Novel Methods & Tools:**
- High-level analysis
- Verification
- Micro-reconfiguration (dynamic circuit specialization)
- Runtime support / resource management (for power, area, reconfiguration execution time, ...)

**Expected results:**
- 20% productivity improvement: implementation & verification of dynamically changing systems
- 50% total ownership cost reduction: Network Intrusion Detection & Reverse Time Migration Apps
- 2x performance improvement under power constraints for Global Illumination App

**Early Results:**
- PDR-X: Partial Dynamic Reconfiguration on Maxeler Architectures (HiPEAC Technology Transfer Award)
- GUI for System Specification & Reconfiguration Management
- Runtime system: PCI-based high-speed partial & dynamic reconfiguration

**Analysis**

**Tools for High-Level Analysis:**
- Use Application Task/Dataflow Graph
- Identify Static/Dynamic HW parts & modules
- Analytical model for possible implementations
- Estimate speed, area, power

**Output:**
- Partitioned specification in HW/SW components
- Implementation(s) of HW accelerated modules
- Reconfigurability level: none, region, micro
- Power, Floorplanning, Placement constraints
- A baseline schedule for application execution

**Verification**

Symbolic simulation + equivalence checking
- Compare source & target designs
- Use symbolic simulation
- Simulate w/ symbolic inputs:
  - Match => equivalence
  - Otherwise => found counter example!!!

**Micro-Reconfiguration**

Fine-grain, dynamic circuit specialization
- Parameterized configurations
- New: parameterized routing infrastructure
- Automatic/manual profiling of different implementations

**Run-Time System**

- Efficiently handles online scheduling & placement
- Supports region-/micro-reconfiguration
- Triggers reconfiguration & initiates task execution
- Non-functional information sources (power, temperature,...)
- Configuration caching & prefetching; relocation

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